**What is claimed is**:

1. A phase locked loop frequency synthesizer, comprising:

a phase comparator for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the two signals;

a loop filter for filtering the phase error signal outputted from the phase comparator and stabilizing the filtered signal, to output a control signal;

a voltage controlled oscillator for controlling frequency gain of a signal outputted in response to the control signal outputted from the loop filter;

a divider for dividing the frequency of the output signal of the voltage controlled oscillator according to a division rate to apply it to the phase comparator as the second signal;

a voltage detector for detecting control voltage from the control signal of the voltage controlled oscillator; and

a controller for calculating a variation in gain characteristics of the voltage controlled oscillator using the control voltage outputted from the voltage detector and the division rate of the divider, and adjusting gain of at least one of the phase comparator, the loop filter and the voltage controlled oscillator, to control gain of a loop composed of the

phase comparator, the loop filter, the voltage controlled oscillator and the divider to be substantially uniform.

2. The phase locked loop frequency synthesizer as claimed in claim 1, wherein the division rate of the divider is set by the controller.

3. The phase locked loop frequency synthesizer as claimed in claim 1, wherein the phase comparator includes a charge pump circuit, and phase gain of the phase comparator is controlled by adjusting a current value of a driving bias current source included in the charge pump circuit.

4. The phase locked loop frequency synthesizer as claimed in claim 1, wherein the loop filter includes a variable gain amplifier, and voltage gain of the loop filter is controlled by adjusting a gain value of the variable gain amplifier.

5. The phase locked loop frequency synthesizer as claimed in claim 1, wherein the voltage detector is composed of an analog-digital converter.

6. The phase locked loop frequency synthesizer as claimed in claim 1, wherein the voltage controlled oscillator includes at

least two voltage controlled oscillators, and one of the voltage controlled oscillators is activated according to a control signal provided by the controller.

7. The phase locked loop frequency synthesizer as claimed in claim 1, wherein the voltage controlled oscillator includes at least one inductor and capacitor that determine a frequency band, and frequency gain of the voltage controlled oscillator is varied by controlling an impedance value of the inductor or capacitor.

8. A method for detecting frequency gain of a voltage controlled oscillator of a phase locked loop frequency synthesizer including a phase comparator for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the two signals, a loop filter for filtering the phase error signal outputted from the phase comparator and stabilizing the filtered signal, to output a control signal, a voltage controlled oscillator for controlling frequency gain of a signal output in response to the control signal outputted from the loop filter, and a divider for dividing the frequency of the output signal of the voltage controlled oscillator according to a division rate to apply it to the phase comparator as the second signal, the method comprising the steps of:

a first step of setting the division rate of the divider to a predetermined first division rate, and detecting control voltage from the control signal;

a second step of setting the division rate of the divider to a predetermined second division rate, and detecting control voltage from the control signal; and

a third step of calculating the frequency gain of the voltage controlled oscillator using the frequency of the first signal, the control voltages detected at the first and second steps, the first and second division rates.

9. The method as claimed in claim 8, wherein the frequency gain of the voltage controlled oscillator is calculated by the following equation;

$$Fin \times (N1-N2)/(V1-V2)$$

where; Fin is the first signal, N1 and N2 denote the first and second division rates, respectively, V1 and V2 represent the control voltages detected at the first and second steps, respectively.

10. A method for detecting frequency gain of a voltage controlled oscillator of a phase locked loop frequency synthesizer including a phase comparator for comparing phases of first and second signals applied thereto with each other and

outputting a phase error signal when there is a phase difference between the two signals, a loop filter for filtering the phase error signal outputted from the phase comparator and stabilizing the filtered signal, to output a control signal, a voltage controlled oscillator for controlling frequency gain of a signal output in response to the control signal outputted from the loop filter, and a divider for dividing the frequency of the output signal of the voltage controlled oscillator according to a division rate to apply it to the phase comparator as the second signal, the method comprising the steps of:

a first step of setting the frequency of the output signal of the voltage controlled oscillator to a predetermined first frequency;

a second step of detecting control voltage from the control signal;

a third step of controlling the division rate of the divider to vary the frequency of the output signal of the voltage controlled oscillator by a predetermined frequency value, and detecting control voltage from the control signal;

a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages detected at the second and third steps and the predetermined frequency value; and

a fifth step of comparing the frequency of the output signal of the voltage controlled oscillator with a predetermined second frequency and repeatedly performing the second and fourth steps until the frequency of the output signal has a value identical to the second frequency value.

11. The method as claimed in claim 10, wherein the frequency gain of the voltage controlled oscillator is calculated by the following equation;

Fstep/(V1-V2)

Where; Fstep is the predetermined frequency, V1 denotes the control voltage detected at the second step, and V2 represents the control voltage detected at the third step.

12. A method for detecting frequency gain of a voltage controlled oscillator of a phase locked loop frequency synthesizer including a phase comparator for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the two signals, a loop filter for filtering the phase error signal outputted from the phase comparator and stabilizing the filtered signal, to output a control signal, a voltage controlled oscillator for controlling frequency gain of a signal output in response to the control signal outputted from the loop

filter, and a divider for dividing the frequency of the output signal of the voltage controlled oscillator according to a division rate to apply it to the phase comparator as the second signal, the method comprising the steps of:

a first step of detecting a control voltage value from the control signal at a predetermined reference frequency;

a second step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by a predetermined specific frequency and detecting control voltage from the control signal;

a third step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by the specific frequency and detecting control voltage from the control signal; and

a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages respectively detected at the second and third steps and the frequency of the output signal.

13. The method as claimed in claim 11, wherein the frequency gain of the voltage controlled oscillator is calculated by the following equation;

$$(F1-F2)/(V1-V2)$$

where; F1 is the frequency of the output signal at the second step, F2 is the frequency of the output signal at the third step, V1 denotes the control voltage detected at the second step, and V2 represents the control voltage detected at the third step.

14. A method for controlling a loop gain of a voltage controlled oscillator of a phase locked loop frequency synthesizer including a phase comparator for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the two signals, a loop filter for filtering the phase error signal outputted from the phase comparator and stabilizing the filtered signal, to output a control signal, a voltage controlled oscillator for controlling frequency gain of a signal output in response to the control signal outputted from the loop filter, and a divider for dividing the frequency of the output signal of the voltage controlled oscillator according to a division rate to apply it to the phase comparator as the second signal, the method comprising the steps of:

a first step of setting the frequency of the output signal of the voltage controlled oscillator to a predetermined first frequency;

a second step of detecting control voltage from the control signal;

a third step of controlling the division rate of the divider to vary the frequency of the output signal of the voltage controlled oscillator by a predetermined frequency value, and detecting control voltage from the control signal;

a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages detected at the second and third steps and the predetermined frequency value;

a fifth step of comparing the frequency of the output signal of the voltage controlled oscillator with a predetermined second frequency and repeatedly performing the second and fourth steps until the frequency of the output signal has a value identical to the second frequency value; and

a sixth step of setting a desired output signal frequency of the voltage controlled oscillator, grasping the frequency gain of the voltage controlled oscillator at the corresponding frequency as a value calculated through the first to fifth steps, and controlling gains of the phase comparator and loop filter.

15. The method as claimed in claim 14, wherein the frequency gain of the voltage controlled oscillator is calculated by the following equation;

Fstep/(V1-V2)

Where; Fstep is the predetermined frequency, V1 denotes the control voltage detected at the second step, and V2 represents the control voltage detected at the third step.

16. A method for controlling loop gain of a voltage controlled oscillator of a phase locked loop frequency synthesizer including a phase comparator for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the two signals, a loop filter for filtering the phase error signal outputted from the phase comparator and stabilizing the filtered signal, to output a control signal, a voltage controlled oscillator for controlling frequency gain of a signal output in response to the control signal outputted from the loop filter, and a divider for dividing the frequency of the output signal of the voltage controlled oscillator according to a division rate to apply it to the phase comparator as the second signal, the method comprising the steps of:

a first step of detecting a control voltage value from the control signal at a predetermined reference frequency;

a second step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency

by a predetermined specific frequency and detecting control voltage from the control signal;

a third step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by the specific frequency and detecting control voltage from the control signal;

a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages respectively detected at the second and third steps and the frequency of the output signal; and

a fifth step of controlling gain of the phase comparator or gain of the loop filter, to control the loop gain to be substantially uniform.

17. The method as claimed in claim 16, wherein the frequency gain of the voltage controlled oscillator is calculated by the following equation;

$(F1-F2)/(V1-V2)$

where; F1 is the frequency of the output signal at the second step, F2 is the frequency of the output signal at the third step, V1 denotes the control voltage detected at the second step, and V2 represents the control voltage detected at the third step.

18. A method for controlling frequency gain of a voltage controlled oscillator of a phase locked loop frequency synthesizer to be substantially uniform, the frequency synthesizer including a phase comparator for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the two signals, a loop filter for filtering the phase error signal outputted from the phase comparator and stabilizing the filtered signal, to output a control signal, a voltage controlled oscillator for controlling frequency gain of a signal output in response to the control signal outputted from the loop filter, and a divider for dividing the frequency of the output signal of the voltage controlled oscillator according to a division rate to apply it to the phase comparator as the second signal, the method comprising the steps of:

a first step of detecting a control voltage value from the control signal at a predetermined reference frequency;

a second step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by a predetermined specific frequency and detecting control voltage from the control signal;

a third step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency

by the specific frequency and detecting control voltage from the control signal;

a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages respectively detected at the second and third steps and the frequency of the output signal; and

a fifth step of comparing the calculated frequency gain with a predetermined reference gain and controlling the frequency gain of the voltage controlled oscillator to be substantially uniform.

19. The method as claimed in claim 16, wherein the frequency gain of the voltage controlled oscillator is calculated by the following equation;

$$(F1-F2)/(V1-V2)$$

where; F1 is the frequency of the output signal at the second step, F2 is the frequency of the output signal at the third step, V1 denotes the control voltage detected at the second step, and V2 represents the control voltage detected at the third step.